Dmitry Podvalny

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Experience Summary

20 years in the SW development industry as an engineer and an engineering manager. Vast experience in development and verification of software development tools including simulators, assemblers, linkers, c-compilers, Eclipse based IDEs.

Have a track record of supplying high quality products and fully operational development tools.

Have patents in SW and HW fields.

Experience

Compiler team leader.
2012-now

Toga Networks (Huawei R&D), Hod HaSharon, Israel
Responsible for the development of the toolchain for in-house DSP architecture. Including state-of-the-art highly optimal gcc-based c/c++ compiler, linker, standard libraries.
Outstanding accomplishments:
1. Creation of a configurable infrastructure allowing easy adoption of the whole toolchain to the new architectures.
2. Achieving performance better than of competitors.
3. Improvement of the different compiler optimizations algorithms including software pipelining algorithm/loop unrolling, scheduler.
4. Introduction of new compiler optimizations such as optimization for usage of dual arithmetic units with different pipeline behavior.

Principal SW engineer
2008-2012

LSI, Rosh Ha'ayin, Israel
Tools development for the definition of the next processor architecture. Tools included SQL based environment for the architecture definition, configurable simulator, and assembler.

Team manager
2005 – 2008

LSI, Rosh Ha'ayin, Israel
Group responsibilities included the verification and customer support of the development tools consisting of eclipse based IDE, C compiler, gdb based debugger, simulator, emulator.

Team manager
2003 – 2005

StarCore LLC, Rosh Ha'ayin, Israel
Group responsibilities included development of back-end of the C compiler (low level optimizations), assembly optimizer, assembler, linker, binary utilities for the Starcore DSP processor. Defined, developed and integrated the tools to the 3-rd party (Greenhills) toolchain.

Team manager
2000 – 2003

Infineon Technologies AG, Tel-Aviv, Israel
Group responsibilities included development of the assembler, linker, binary utilities for Carmel DSP processor.

SW engineer
1997 – 2000

I.C.COM
Main Projects:
Assembler for the Carmel DSP processor. Emulation module for the development board. Self-testing system for the development board.

Education

BA and MA degrees in Mathematics and computer science.

MA, Mathematics and Computer science

Haifa university, Israel
Thesis on DSM (distributed shared memory over network) system with ParC (parallel C) compiler. Work included definition of the new invalidation protocol (YInvalidate) for DSM system, development of the C compiler and implementation of low-level DSM library supporting different protocols.

BA, Mathematics and computer science

Haifa University, Israel