Hardware Engineer

Verification / CHIP / VLSI / Logic Design / FPGA

**Yotam Koren**

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**Summary**

* **2+ years** of experience as **Chip Design Verification Engineer** and **FPGA + Firmware Engineer** at **Inuitive,** and **Elta Systems**.
* Proficiency in **SystemVerilog** and experience with both coverage-driven verification using **UVM** and the **Formal Verification** tool of **JasperGold**,Using **SVA**.
* Experience in a **Hardware verification flow** of **complex designs (full chip** and **block-level)** from **test plan** definition to execution.
* Skilled in **scripting languages** such as **Perl/Python**, with the ability to **automate verification** processes.
* Solid understanding of **RTL design**, coupled with strong **debugging**, problem-solving, and **analytical skills.**
* **B.Sc. Electrical Engineering**, Ben Gurion University
* I am passionate about **Engineering** since I was **16 years old**: I participated in a **gifted teenagers program** at **Weizmann Institute**.

**Experience**

2022 - Present **Chip Design Verification Engineer**, **Inuitive**

***The Vision-on-Chip processors company***

* Using: **Verilog**, **SystemVerilog**, **UVM**, **C,** DVE simulation tool, **Linux**.

LPDDR Project:

* **Block Level** verification environment including integration of Verification IPs: **APB, AXI, Synopsys LPDDR Memory.** Also, register and memory virtual models.
* Configuring **DDR Controller** and **PHY** for PHY firmware tests to optimize the DDR memory chip functionality.
* Simulating host CPUs communications with the device.

OTP Project:

* **Block Level** verificationof a module communicating with a non-volatile memory, which is responsible for hardware security and data protection.

Chip-level Projects:

* **Chip-level environments** for many modules and domains around the chip (**hardware accelerators,** cores, memories, integrated IPs, etc). Complex system-level understanding of the chip functionality.
* **Formal Verification** tool of **JasperGold**.Using **SVA** for complex model checking.
* **Gate-level** simulations**, debugging**, and root cause analysis.

2020 - 2021 **Hardware Design - FPGA / Firmware**, **Elta Systems**

* **Multidisciplinary product** of HW and SW in the fields of **FPGA**, **RTL**, **VHDL**, **C**, **Firmware**, Real Time Embedded, ARM processor, and signal processing.
* Implementing a **Multiprocessor system on a chip** (**MP Soc**) platform. Creating an efficient interface between components on the chip - **ARM processor, FPGA, DDR memory.**
* Coding with: **VHDL** for **FPGA (using Xilinx Vivado),** and **C** to run on processor **(using Xilinx SDK).**
* Real-time Signal processing optimization.

**Education**

2017 - 2021 **B.Sc. Electrical Engineering**, Ben Gurion University.

* Majored in Computers Engineering and **VLSI**

2010 - 2011 Ahad Ha’am High School, **GPA: 113**

* **Gifted students program,** Weizmann Institute - **Biometric Sensor Project - Final Grade 100**

**Skills**

**Verilog, SystemVerilog**, **UVM, Formal Verification**, **SVA, JasperGold**, **FPGA,** RTL, **VHDL, C, Python, Perl,** DVE, **Linux, MATLAB,** Quartus, ModelSim, **MARS,** Xilinx Vivado, **Xilinx SDK**.

**Military Service**

2011 - 2014 Combat Soldier at Nahal Brigade, Position Commander Assistant

**Volunteer Work**

2009 - 2010 **"Young Ambassadors" program** that provides tools for the young ambassador, including Speeches in front of ministry officials